The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC632

Reconfigurable FPGA

with 64 TTL I/O / 32 Differential I/O Lines

Version 1.0

User Manual

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TPMC632-10R

64 TTL I/O Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-11R

32 Differential I/O Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-12R

32 TTL and 16 Differential I/O Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-13R

32 Differential M-LVDS Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-14R

32 TTL and 16 Differential M-LVDS Lines, XC6SLX45T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-20R

64 TTL I/O Lines, XC6SLX100T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-21R

32 Differential I/O Lines, XC6SLX100T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-22R

32 TTL and 16 Differential I/O Lines, XC6SLX100T-2 Spartan-6 FPGA,128 MB DDR3

TPMC632-23R

32 Differential M-LVDS Lines, XC6SLX100T-2 Spartan-6 FPGA ,128 MB DDR3

TPMC632-24R

32 TTL and 16 Differential M-LVDS Lines, XC6SLX100T-2 Spartan-6 FPGA ,128 MB DDR3

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‘Active Low’ is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0.0	Initial Issue	January 2012
1.0.1	Four further board variants with M-LVDS I/O buffers are created	January 2013
1.0.2	Added chapter “Known Issue”	May 2013
1.0.3	Added DDR3 SDRAM Alternative Part	May 2015
1.0.4	Added SPI-Flash Alternative Part	September 2015

Table of Contents

1 PRODUCT DESCRIPTION 7
2 TECHNICAL SPECIFICATION 8
3 HANDLING AND OPERATION INSTRUCTION 10
3.1 ESD Protection 10
3.2 Thermal Considerations 10
4 FUNCTIONAL DESCRIPTION 11
4.1 FPGA Block Diagram 11
4.2 FPGA 12
4.3 Gigabit Transceiver (GTP) 13
4.4 Configuration 14
4.4.1 Selecting the Configuration Source 14
4.4.2 JTAG 15
4.4.3 Board Configuration CPLD 15
4.4.4 Programming Configuration devices 16
4.5 Clocking 17
4.5.1 FPGA Clock Sources 17
4.6 I/O Interface 18
4.7 Memory 22
4.7.1 DDR3 SDRAM 22
4.7.2 SPI-Flash 24
4.8 User GPIO 25
4.9 On Board Indicators 26
4.10 Thermal Management 26
5 DESIGN HELP 27
5.1 Example Design 27
6 INSTALLATION 28
6.1 Pull Up Voltage 28
6.2 I/O Interface 29
6.2.1 TTL I/O Interface 29
6.2.2 Differential I/O Interface 30
6.2.3 Multipoint-LVDS Interface 30
6.3 Back I/O Configuration 31
6.4 FPGA Debug Connector 33
6.4.1 Connecting TA900 to TPMC632 Debug Connector 33
6.5 FPGA JTAG Connector 34
7 PIN ASSIGNMENT – I/O CONNECTOR 35
7.1 Overview 35
7.2 X1 Front Panel I/O Connector 35
7.2.1 Connector Type 35
7.2.2 Pin Assignment 36
7.3 Back I/O PMC Connector P14 37
7.3.1 Connector Type 37
7.3.2 Pin Assignment 37
7.4 X2 JTAG Header 39
7.4.1 Connector Type 39
7.4.2 Pin Assignment 39

7.5 X3 Debug-Connector 40
7.5.1 Connector Type 40
7.5.2 Pin Assignment 40
8 KNOWN ISSUES 41
9 APPENDIX A 42

List of Figures

FIGURE 1-1 : BLOCK DIAGRAM 7
FIGURE 4-1 : FPGA BLOCK DIAGRAM 11
FIGURE 4-2 : GTP BLOCK DIAGRAM 13
FIGURE 4-3 : CONFIGURATION SOURCE SELECTION 14
FIGURE 4-4 : CONFIGURATION DIP-SWITCH SETTINGS 14
FIGURE 4-5 : JTAG-CHAIN 15
FIGURE 4-6 : CONFIGURATION DIP-SWITCH SETTINGS 15
FIGURE 4-7 : FPGA CLOCK SOURCES 17
FIGURE 6-1 : PULL (UP) VOLTAGE JUMPER SETTING 28
FIGURE 6-2 : TTL I/O INTERFACE 29
FIGURE 6-3 : DIFFERENTIAL I/O INTERFACE 30
FIGURE 6-4 : M-LVDS I/O INTERFACE 30
FIGURE 6-5 : JUMPER POSITIONS FOR GROUND OPTION 31
FIGURE 6-6 : JUMPER POSITIONS FOR BACK I/O OPTIONS 32
FIGURE 6-7 : DEBUG CONNECTOR X3 33
FIGURE 6-8 : FPGA JTAG CONNECTOR X2 34
FIGURE 7-1 : FRONT PANEL I/O CONNECTOR NUMBERING 35

List of Tables

TABLE 2-1 : TECHNICAL SPECIFICATION 9
TABLE 4-1 : TPMC632 FPGA FEATURE OVERVIEW 12
TABLE 4-2 : FPGA BANK USAGE 12
TABLE 4-3 : GTP CONNECTIONS 13
TABLE 4-4 : MULTI GIGABIT TRANSCEIVER REFERENCE CLOCKS 13
TABLE 4-5 : AVAILABLE FPGA CLOCKS 17
TABLE 4-6 : DIGITAL I/O INTERFACE 21
TABLE 4-7 : DDR3 SDRAM INTERFACE 23
TABLE 4-8 : FPGA SPI-FLASH CONNECTIONS 24
TABLE 4-9 : FPGA GENERAL PURPOSE I/O 25
TABLE 4-10: BOARD-STATUS AND USER LEDS 26
TABLE 7-1 : PIN ASSIGNMENT FRONT PANEL I/O CONNECTOR X1 36
TABLE 7-2 : PIN ASSIGNMENT BACK I/O PMC CONNECTOR P14 38
TABLE 7-3 : PIN ASSIGNMENT JTAG HEADER X2 39
TABLE 7-4 : PIN ASSIGNMENT DEBUG CONNECTOR X3 40

1 Product Description

The TPMC632 is a standard single-width 32 bit PMC module providing a user configurable XC6SLX45T-2 or XC6SLX100T-2 Spartan-6 FPGA. The integrated Spartan-6's PCIe Endpoint Block is connected to a PCIe-to-PCI Bridge which routed to the PMC PCI Interface.

Different variants of the TPMC632 provide ESD-protected TTL lines, ESD-protected differential I/O lines and differential Multipoint-LVDS lines. Also combination of 32 TTL and 16 differential I/O lines are supported.

All lines are individually programmable as input, output or tri-state. The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs. Each TTL I/O line has a pull resistor. The pull voltage level is selectable to be either +3.3V, +5V and additionally GND. The differential I/O lines are terminated by 120Ω resistors and the differential Multipoint-LVDS lines are terminated by 100Ω resistors.

The FPGA is connected to a 128 Mbytes, 16 bit wide DDR3 SDRAM. As SDRAM-interface a hardwired internal Memory Controller Block of the Spartan-6 is used.

The FPGA is configured by a platform flash or SPI flash. The flash device is in-system programmable. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx "ChipScope").

The TPMC632 provides either front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14.

User applications for the TPMC632 with XC6SLX45T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com. The larger FPGA densities require a full licensed ISE Design Suite.

TEWS offers an FPGA Development Kit (TPMC632-FDK) which consists of well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TPMC632. It implements a DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream.

Please note: The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available).

Software Support (TPMC632-SW-xx) for different operating systems is available.

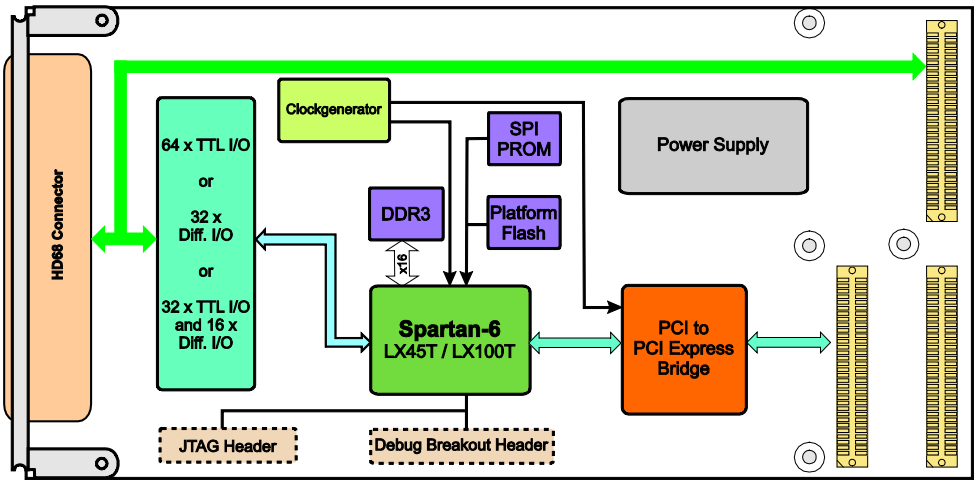


Figure 1-1 : Block Diagram

2 Technical Specification

<table>
<tr><td colspan="2">PMC Interface</td></tr>
<tr><td>Mechanical Interface</td><td>PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1
Single Size</td></tr>
<tr><td>Electrical Interface</td><td>PCI Rev. 3.0 compliant
33 MHz or 66 MHz / 32 bit PCI
3.3V and 5V PCI Signaling Voltage</td></tr>
<tr><td colspan="2">On Board Devices</td></tr>
<tr><td>PCI to PCI Express Bridge</td><td>PEX8112 (PLX Technology)</td></tr>
<tr><td>PCI Express Endpoint</td><td>Spartan-6 PCI Express Endpoint Block</td></tr>
<tr><td>User configurable FPGA</td><td>TPMC632-1xR: XC6SLX45T-2 (Xilinx)
TPMC632-2xR: XC6SLX100T-2 (Xilinx)</td></tr>
<tr><td>Configuration Flash</td><td>TPMC632-1xR: XCF16P (Xilinx)
TPMC632-2xR: XCF32P (Xilinx)</td></tr>
<tr><td>SPI-Flash</td><td>W25Q32 (Winbond) 32 Mbit (can be used for FPGA configuration)
W25Q32 (Winbond) 32 Mbit (contains TPMC632 FPGA Example)</td></tr>
<tr><td>DDR3 RAM</td><td>MT41J64M16 or MT41K64M16 (Micron) 64 Meg x 16 Bit</td></tr>
<tr><td colspan="2">I/O Interface</td></tr>
<tr><td>Number of Channels</td><td>TPMC632-x0R: 64 ESD-protected TTL lines
TPMC632-x1R: 32 differential I/O lines
TPMC632-x2R: 32 TTL and 16 differential I/O lines
TPMC632-x3R: 32 M-LVDS I/O lines
TPMC632-x4R: 32 TTL and 16 M-LVDS I/O lines.

TTL signaling voltage level (maximum current:+/-32 mA),
EIA-422/-485 signaling level or
M-LVDS Standard (TIA/EIA-899)</td></tr>
<tr><td>I/O Connector</td><td>Front I/O HD68 SCSI-3 type Connector
(AMP 787082-7 or compatible)
PMC P14 I/O (64 pin Mezzanine Connector)</td></tr>
<tr><td colspan="2">Physical Data</td></tr>
<tr><td>Power Requirements</td><td>Depends on FPGA design
With TPMC632 FPGA Example Design / without external load
<table>
<tr><td></td><td colspan="2">typical @ +3.3V DC</td><td colspan="2">typical @ +5.0V DC</td></tr>
<tr><td>Output</td><td>disable</td><td>enable</td><td>disable</td><td>drive low</td></tr>
<tr><td>TPMC632-x0R</td><td>860mA</td><td>900mA</td><td><5mA</td><td>72mA</td></tr>
<tr><td>TPMC632-x1R</td><td>860mA</td><td>1600mA</td><td><5mA</td><td><5mA</td></tr>
<tr><td>TPMC632-x2R</td><td>860mA</td><td>1260mA</td><td><5mA</td><td>36mA</td></tr>
<tr><td>TPMC632-x3R</td><td>640mA</td><td>640mA</td><td><5mA</td><td><5mA</td></tr>
<tr><td>TPMC632-x4R</td><td>860mA</td><td>980mA</td><td><5mA</td><td>36mA</td></tr>
</table></td></tr>
</table>

Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPMC632-10R/-20R: 291000 h TPMC632-11R/-21R: 336000 h TPMC632-12R/-22R: 311000 h TPMC632-13R/-23R: 324000 h TPMC632-14R/-24R: 306000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TPMC632-xxR: 126 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instruction

3.1 ESD Protection

The TPMC632 is sensitive to static electricity. Packing, unpacking and all other handling of the TPMC632 has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is recommended during operation. Without forced air cooling, damage to the device can occur.

4 Functional Description

4.1 FPGA Block Diagram

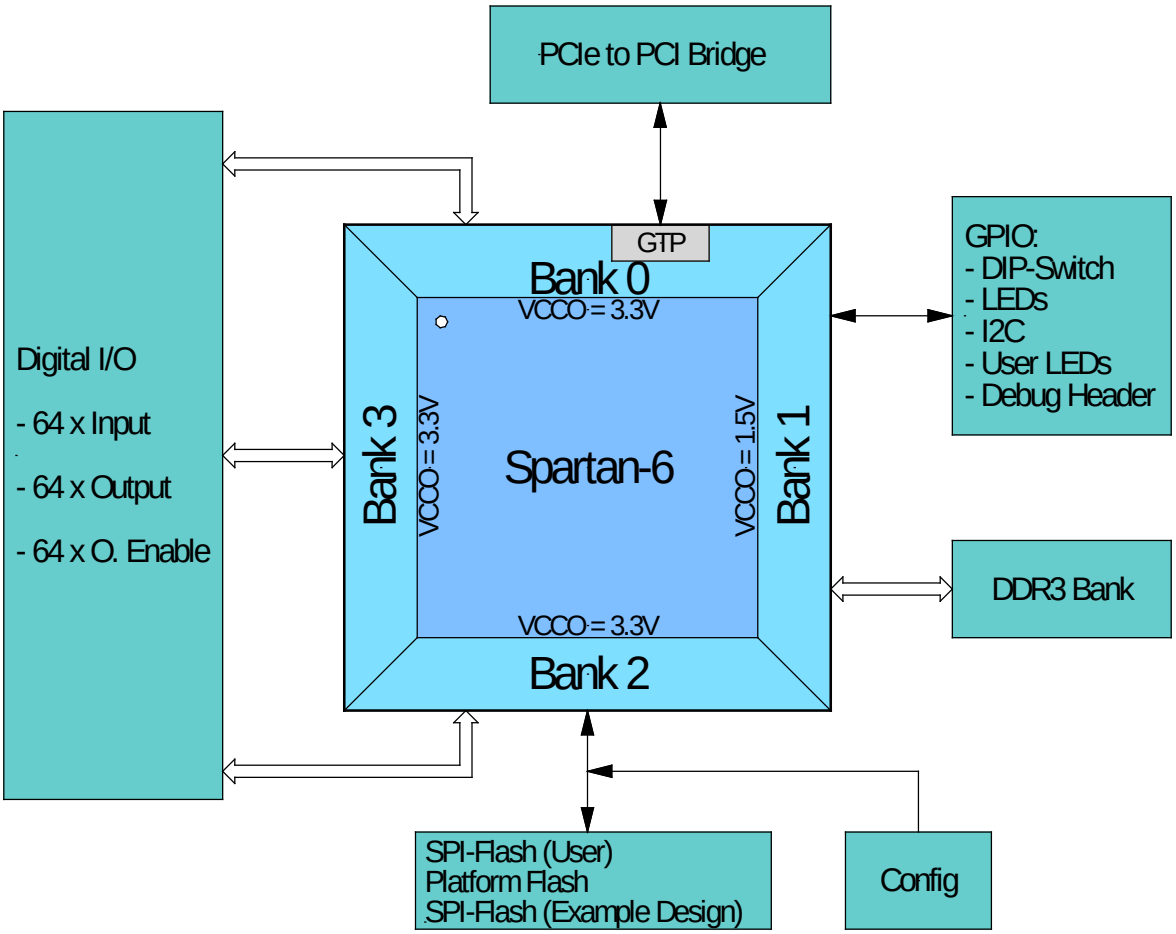


Figure 4-1 : FPGA Block Diagram

4.2 FPGA

The FPGA is a Spartan-6 LX45T-2 or LX100T-2 FPGA. Each Spartan-6 FPGA in a FGG484 package provides two Memory Controller Blocks and one Endpoint Block for PCI Express (x1 Linkage).

Spartan-6	Slices	Flip-Flops	DSP48A1 Slices	Block RAM (Kb)	CMTs	GTP Transceivers
LX45T	6.822	54.576	58	2.088	4	4
LX100T	15.822	126.576	180	4.824	6	4

Table 4-1 : TPMC632 FPGA Feature Overview

The board supports JTAG, master serial mode configuration from SPI-Flash or SelectMAP configuration from a Platform Flash.

The FPGA is equipped with 4 I/O banks and 4 GTP transceivers.

Bank	V_{CCO}	V_{REF}	Signals	Remarks
Bank 0	3.3V	none	dig. I/O Interface	
Bank 1	1.5V	0.75V	DDR3 Bank	+GPIO / LED /Debug
Bank 2	3.3V	none	dig. I/O Interface	+Configuration
Bank 3	3.3V	none	dig. I/O Interface	
GTP Bank	**Description**			**Remarks**
GTP101	PCIe Endpoint Block			Lane 0
GTP101	not used			Lane 1
GTP123	not used			Lane 0
GTP123	not used			Lane 1

Table 4-2 : FPGA Bank Usage

The FPGA's VCCAUX is connected to the 3.3V supply.

4.3 Gigabit Transceiver (GTP)

The TPMC632 provides one GTP as Spartan-6 PCI Express Endpoint Block.

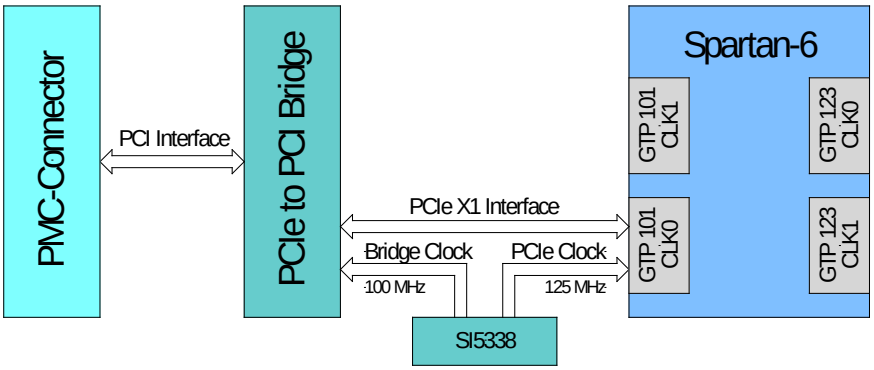


Figure 4-2 : GTP Block Diagram

GTP	Signal	FPGA Pins	Connected to
MGT0_101	MGTTX	B6 / A6	used for PCI Express Endpoint Block
	MGTRX	D7 / C7	
MGT1_101	MGTTX	B8 / A8	not used
	MGTRX	D9 / C9	
MGT0_123	MGTTX	B14 / A14	not used
	MGTRX	D13 / C13	
MGT1_123	MGTTX	B16 / A16	not used
	MGTRX	D15 / C15	

Table 4-3 : GTP Connections

The GTP clock MGT0_101 (PCI Express Endpoint Block clock reference) of 125 MHz is generated by the SI5338 low-jitter clock generator.

MGT1_101, MGT0_123 and MGT1_123 are not used on the TPMC632.

GTP	Signal	FPGA Pins	Connected to
MGT0_101	MGTREFCLK	A10 / B10	125 MHz (derived SI5338 clock generator)
MGT1_101	MGTREFCLK	C11 / D11	not used
MGT0_123	MGTREFCLK	A12 / B12	not used
MGT1_123	MGTREFCLK	E12 / F12	not used

Table 4-4 : Multi Gigabit Transceiver Reference Clocks

4.4 Configuration

The FPGA can be configured by the following sources:

- Platform Flash
- SPI-Flash
- JTAG

The configuration flash can be selected with a DIP-switch; alternatively, JTAG configuration is always available. For the XILINX Platform Flash configuration the Master SelectMAP/BPI mode with 8bit bus width is used. The SPI-Flash configuration uses the Master Serial / SPI mode. Both flashes could be programmed via JTAG; the SPI-Flash uses the indirect SPI programming mode.

To change the TPMC632 programming, JTAG-capable hardware is needed (i.e. the Xilinx Platform Cable USB II).

On delivery the configuration Platform Flash and the User SPI-Flash (USER Flash) are blank.

A second SPI-Flash (TEWS Flash) is factory programmed with the TPMC632 Platform Example Application.

4.4.1 Selecting the Configuration Source

Besides direct JTAG configuration, the TPMC632 provides two user configuration sources: a platform flash and a SPI-Flash. Both devices share common pins, so a selection must be made. With the Configuration DIP switch the Configuration source could be selected.

Set the Configuration DIP Switch S1 to ON, the SPI Flash interface is selected, with Configuration DIP Switch S1 set to OFF the FPGA will configure from the Platform Flash.

Set the Configuration DIP Switch S2 to ON the SPI Flash A (USER Flash) is selected. Set the Configuration DIP Switch S2 to OFF the SPI Flash B (TEWS Flash) is selected.

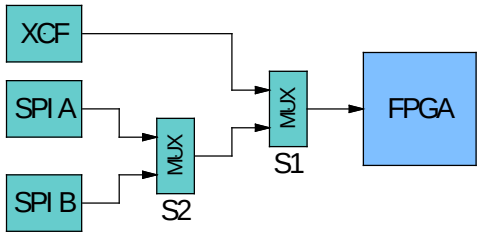


Figure 4-3 : Configuration Source Selection

After configuration the SPI-Flash A is always user accessible, regardless of the switch setting.

Switch	Signal	Description
S1	ON	Configure FPGA from SPI Flash
	OFF	Configure FPGA from Platform Flash
S2	ON	SPI Flash A (USER Flash) selected
	OFF	SPI Flash B (TEWS Flash) selected

Figure 4-4 : Configuration DIP-Switch Settings

4.4.2 JTAG

The JTAG-chain is accessible from the JTAG Header, from the Debug Connector or from the PMC-Interface. These interfaces are connected in parallel, so only one connection should be made to avoid signal contentions/possible hardware damage.

For direct FPGA configuration, FPGA readback or in-system diagnostics with ChipScope, the JTAG Header can be used to access the JTAG-chain. The JTAG-chain can be extended to include the TPMC632 configuration CPLD.

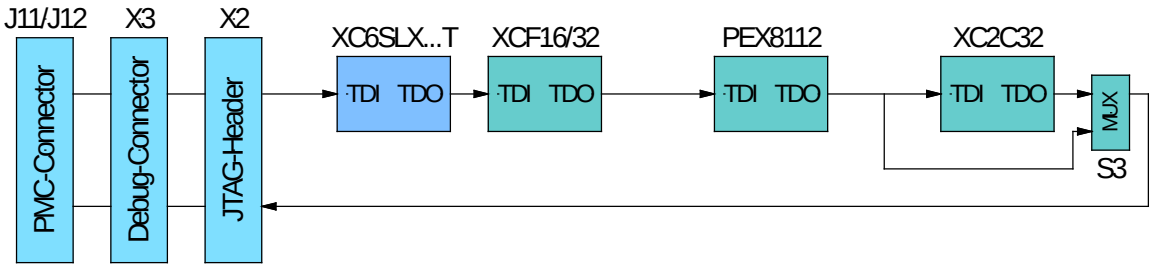


Figure 4-5 : JTAG-Chain

S3	ON	Include configuration CPLD to JTAG chain.
	OFF	Bypass configuration CPLD (default)
S4	ON	Not used
	OFF	

Figure 4-6 : Configuration DIP-Switch Settings

4.4.3 Board Configuration CPLD

The Board Configuration CPLD (BCC) is factory configured, and handles the basic board setup.

Changing or erase the BCC content leads to an inoperable TPMC632 FPGA configuration.

4.4.4 Programming Configuration devices

Both user configuration devices XILINX Platform Flash and SPI Flash could be programmed via JTAG interface. The second SPI Flash (TEWS Flash) could not be programmed.

For programming the configuration devices the XILINX programming tool iMPACT can be used. An addition JTAG programming hardware is needed (i.e. the Xilinx Platform Cable USB II).

To use the maximum configuration speed, the TPMC632 must be configured to use the 32 MHz external master clock as CCLK. To use these configuration feature, the configuration option 'Enable External Master Clock' (-g ExtMasterCclk_en) must be enabled. Without this option, the configuration time for the Spartan6 FPGA exceed the maximum PCI bus setup time.

TPMC632-1xR configuration devices:

SPI Flash: Winbond W25Q32BV or W25Q32FV; 32M; Data Width = 4bit

XILINX Flash/PROM: XCF16P; 16M; parallel mode

TPMC632-2xR configuration devices:

SPI Flash: Winbond W25Q32BV or W25Q32FV; 32M; Data Width = 4bit

XILINX Flash/PROM: XCF32P; 32M; parallel mode

4.5 Clocking

4.5.1 FPGA Clock Sources

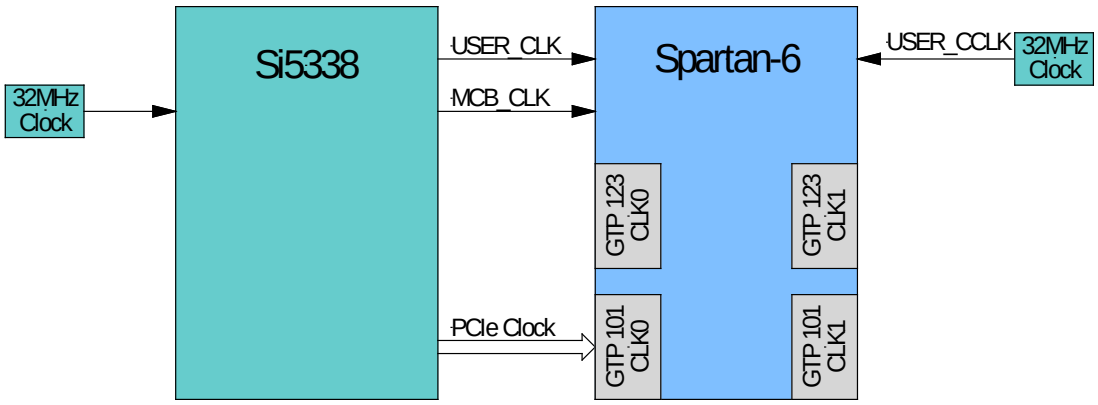


Figure 4-7 : FPGA Clock Sources

The following table lists the available clock sources on the TPMC632:

FPGA Clock-Pin Name	FPGA Pin Number	Source	Description
MGTREFCLK0_101	A10 / B10	SI5338 low-jitter clock generator	125 MHz PCIe Reference clock
IO_L30P_GCLK1_D13_2	Y13	SI5338 low-jitter clock generator	MCB CLK 62.5 MHz
IO_L29N_GCLK2_2	U12	SI5338 low-jitter clock generator	USER CLK 83.3325 MHz
IO_L30N_GCLK0_USERCCLK_2	AB13	32MHz, 3,3V oscillator	Used for external configuration clock (CCLK) After configuration this clock could be used by FPGA design.

Table 4-5 : Available FPGA clocks

4.6 I/O Interface

Each of the 64 digital IO channels are realized with single ended or differential digital buffers. Each channel provides an input; output and an output enable signal which is direct connected to the FPGA device.

The IO channels are accessible through the IO Bank 0, Bank 2 and Bank 3 of the Spartan-6 FPGA. The subsequent table lists required I/O setting for correct interfacing.

Signal Name	Pin Number	Direction	IO Standard	IO Bank	Drive [mA]	Slew Rate
FPGA_IN<0>#	L4	INPUT	LVCMOS33	3		
FPGA_IN<1>#	M3	INPUT	LVCMOS33	3		
FPGA_IN<2>#	M4	INPUT	LVCMOS33	3		
FPGA_IN<3>#	M5	INPUT	LVCMOS33	3		
FPGA_IN<4>#	N4	INPUT	LVCMOS33	3		
FPGA_IN<5>#	P3	INPUT	LVCMOS33	3		
FPGA_IN<6>#	L1	INPUT	LVCMOS33	3		
FPGA_IN<7>#	L3	INPUT	LVCMOS33	3		
FPGA_IN<8>#	V17	INPUT	LVCMOS33	2		
FPGA_IN<9>#	W18	INPUT	LVCMOS33	2		
FPGA_IN<10>#	Y17	INPUT	LVCMOS33	2		
FPGA_IN<11>#	V15	INPUT	LVCMOS33	2		
FPGA_IN<12>#	W17	INPUT	LVCMOS33	2		
FPGA_IN<13>#	Y18	INPUT	LVCMOS33	2		
FPGA_IN<14>#	V2	INPUT	LVCMOS33	3		
FPGA_IN<15>#	Y1	INPUT	LVCMOS33	3		
FPGA_IN<16>#	Y14	INPUT	LVCMOS33	2		
FPGA_IN<17>#	Y15	INPUT	LVCMOS33	2		
FPGA_IN<18>#	B2	INPUT	LVCMOS33	0		
FPGA_IN<19>#	C3	INPUT	LVCMOS33	0		
FPGA_IN<20>#	A4	INPUT	LVCMOS33	0		
FPGA_IN<21>#	D4	INPUT	LVCMOS33	0		
FPGA_IN<22>#	H14	INPUT	LVCMOS33	0		
FPGA_IN<23>#	D5	INPUT	LVCMOS33	0		
FPGA_IN<24>#	E5	INPUT	LVCMOS33	0		
FPGA_IN<25>#	E6	INPUT	LVCMOS33	0		
FPGA_IN<26>#	A19	INPUT	LVCMOS33	0		
FPGA_IN<27>#	F16	INPUT	LVCMOS33	0		
FPGA_IN<28>#	A2	INPUT	LVCMOS33	0		
FPGA_IN<29>#	D3	INPUT	LVCMOS33	0		
FPGA_IN<30>#	B20	INPUT	LVCMOS33	0		
FPGA_IN<31>#	F8	INPUT	LVCMOS33	0		
FPGA_IN<32>#	H11	INPUT	LVCMOS33	0		
FPGA_IN<33>#	H10	INPUT	LVCMOS33	0		
FPGA_IN<34>#	G9	INPUT	LVCMOS33	0		
FPGA_IN<35>#	G8	INPUT	LVCMOS33	0		
FPGA_IN<36>#	B3	INPUT	LVCMOS33	0		
FPGA_IN<37>#	A3	INPUT	LVCMOS33	0		
FPGA_IN<38>#	A18	INPUT	LVCMOS33	0		
FPGA_IN<39>#	B18	INPUT	LVCMOS33	0		

FPGA_IN<40>#	A17	INPUT	LVCMOS33	0		
FPGA_IN<41>#	A5	INPUT	LVCMOS33	0		
FPGA_IN<42>#	C5	INPUT	LVCMOS33	0		
FPGA_IN<43>#	C4	INPUT	LVCMOS33	0		
FPGA_IN<44>#	G13	INPUT	LVCMOS33	0		
FPGA_IN<45>#	G15	INPUT	LVCMOS33	0		
FPGA_IN<46>#	D17	INPUT	LVCMOS33	0		
FPGA_IN<47>#	E16	INPUT	LVCMOS33	0		
FPGA_IN<48>#	G16	INPUT	LVCMOS33	0		
FPGA_IN<49>#	F17	INPUT	LVCMOS33	0		
FPGA_IN<50>#	D18	INPUT	LVCMOS33	0		
FPGA_IN<51>#	D19	INPUT	LVCMOS33	0		
FPGA_IN<52>#	F15	INPUT	LVCMOS33	0		
FPGA_IN<53>#	F9	INPUT	LVCMOS33	0		
FPGA_IN<54>#	C19	INPUT	LVCMOS33	0		
FPGA_IN<55>#	F7	INPUT	LVCMOS33	0		
FPGA_IN<56>#	G11	INPUT	LVCMOS33	0		
FPGA_IN<57>#	F14	INPUT	LVCMOS33	0		
FPGA_IN<58>#	C18	INPUT	LVCMOS33	0		
FPGA_IN<59>#	C17	INPUT	LVCMOS33	0		
FPGA_IN<60>#	A20	INPUT	LVCMOS33	0		
FPGA_IN<61>#	H12	INPUT	LVCMOS33	0		
FPGA_IN<62>#	F10	INPUT	LVCMOS33	0		
FPGA_IN<63>#	H13	INPUT	LVCMOS33	0		
FPGA_OE<0>#	T15	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<1>#	AB16	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<2>#	AB11	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<3>#	AB8	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<4>#	AB10	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<5>#	AB7	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<6>#	W8	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<7>#	AB9	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<8>#	R8	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<9>#	AB4	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<10>#	AB17	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<11>#	AB15	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<12>#	W12	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<13>#	R1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<14>#	V1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<15>#	T7	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<16>#	U6	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<17>#	AB19	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<18>#	C1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<19>#	M8	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<20>#	AA18	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<21>#	AB18	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<22>#	U14	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<23>#	W14	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<24>#	Y16	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<25>#	U16	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<26>#	V13	OUTPUT	LVCMOS33	2	8	SLOW

FPGA_OE<27>#	W13	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<28>#	U1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<29>#	AA1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<30>#	U13	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<31>#	AA2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<32>#	W6	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<33>#	W4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<34>#	R3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<35>#	T6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<36>#	D1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<37>#	V3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<38>#	H5	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<39>#	J6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<40>#	F2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<41>#	G1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<42>#	H2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<43>#	H1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<44>#	U3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<45>#	U4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<46>#	T3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<47>#	P6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<48>#	R7	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<49>#	M7	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<50>#	U8	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OE<51>#	M2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<52>#	T4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<53>#	V5	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<54>#	K1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<55>#	N1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<56>#	P5	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<57>#	N6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<58>#	K2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<59>#	N7	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<60>#	P7	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<61>#	P1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<62>#	K5	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OE<63>#	J4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<0>#	Y3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<1>#	AB14	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<2>#	AB12	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<3>#	AA4	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<4>#	N3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<5>#	W3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<6>#	AA10	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<7>#	Y6	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<8>#	M6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<9>#	L6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<10>#	K4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<11>#	K3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<12>#	P2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<13>#	T1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<14>#	J3	OUTPUT	LVCMOS33	3	8	SLOW

FPGA_OUT<15>#	R4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<16>#	T5	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<17>#	M1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<18>#	D2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<19>#	J7	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<20>#	F1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<21>#	H3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<22>#	G3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<23>#	Y9	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<24>#	Y12	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<25>#	T2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<26>#	E3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<27>#	AA16	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<28>#	Y2	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<29>#	W1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<30>#	K7	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<31>#	K8	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<32>#	H4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<33>#	G4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<34>#	AA8	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<35>#	V7	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<36>#	F3	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<37>#	E4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<38>#	H6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<39>#	G7	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<40>#	E1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<41>#	H8	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<42>#	F5	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<43>#	G6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<44>#	B1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<45>#	W15	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<46>#	K6	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<47>#	P8	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<48>#	R9	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<49>#	V11	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<50>#	Y10	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<51>#	P4	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<52>#	V9	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<53>#	W10	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<54>#	W11	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<55>#	U9	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<56>#	T8	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<57>#	T10	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<58>#	U10	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<59>#	Y7	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<60>#	J1	OUTPUT	LVCMOS33	3	8	SLOW
FPGA_OUT<61>#	U15	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<62>#	R11	OUTPUT	LVCMOS33	2	8	SLOW
FPGA_OUT<63>#	T11	OUTPUT	LVCMOS33	2	8	SLOW

Table 4-6 : Digital I/O Interface

4.7 Memory

The TPMC632 is equipped with a 128 Mbytes, 16 bit wide DDR3 SDRAM and a 32-Mbit non-volatile SPI-Flash. The SPI-Flash can also be used as configuration memory.

4.7.1 DDR3 SDRAM

The TPMC632 provides a MT41J64M16 or MT41K64M16 (96-ball) DDR3 memory device. The memory is accessible through the Memory Controller Block hard-IPs in bank 1 of the Spartan-6 FPGA.

The memory component's CS# is fixed to GND. The address bits A14 and A13 are memory address expansion bits.

Signal	DDR Bank A FPGA Pin	I/O Standard	Termination	Memory Device	
				Pin	Name
A0	H21	SSTL15_II	49.9Ω V_{TT}	N3	A0
A1	H22	SSTL15_II	49.9Ω V_{TT}	P7	A1
A2	G22	SSTL15_II	49.9Ω V_{TT}	P3	A2
A3	J20	SSTL15_II	49.9Ω V_{TT}	N2	A3
A4	H20	SSTL15_II	49.9Ω V_{TT}	P8	A4
A5	M20	SSTL15_II	49.9Ω V_{TT}	P2	A5
A6	M19	SSTL15_II	49.9Ω V_{TT}	R8	A6
A7	G20	SSTL15_II	49.9Ω V_{TT}	R2	A7
A8	E20	SSTL15_II	49.9Ω V_{TT}	T8	A8
A9	E22	SSTL15_II	49.9Ω V_{TT}	R3	A9
A10	J19	SSTL15_II	49.9Ω V_{TT}	L7	A10/AP
A11	H19	SSTL15_II	49.9Ω V_{TT}	R7	A11
A12	F22	SSTL15_II	49.9Ω V_{TT}	N7	A12/BCN
A13	G19	SSTL15_II	49.9Ω V_{TT}	T3	NC/A13
A14	F20	SSTL15_II	49.9Ω V_{TT}	T7	NC/A14
BA0	K17	SSTL15_II	49.9Ω V_{TT}	M2	BA0
BA1	L17	SSTL15_II	49.9Ω V_{TT}	N8	BA1
BA2	K18	SSTL15_II	49.9Ω V_{TT}	M3	BA2
RAS#	K21	SSTL15_II	49.9Ω V_{TT}	J3	RAS#
CAS#	K22	SSTL15_II	49.9Ω V_{TT}	K3	CAS#
WE#	K19	SSTL15_II	49.9Ω V_{TT}	L3	WE#
CS#	-	-	100Ω GND	L2	CS#
RESET#	H18	LVCMOS15	4.7kΩ GND	T2	RESET#
CKE	F21	SSTL15_II	4.7kΩ GND	K9	CKE
ODT	J22	SSTL15_II	49.9Ω V_{TT}	K1	ODT
DQ0	R20	SSTL15_II	ODT	E3	DQ0
DQ1	R22	SSTL15_II	ODT	F7	DQ1

Signal	DDR Bank A FPGA Pin	I/O Standard	Termination	Memory Device	
				Pin	Name
DQ2	P21	SSTL15_II	ODT	F2	DQ2
DQ3	P22	SSTL15_II	ODT	F8	DQ3
DQ4	L20	SSTL15_II	ODT	H3	DQ4
DQ5	L22	SSTL15_II	ODT	H8	DQ5
DQ6	M21	SSTL15_II	ODT	G2	DQ6
DQ7	M22	SSTL15_II	ODT	H7	DQ7
DQ8	T21	SSTL15_II	ODT	D7	DQ8
DQ9	T22	SSTL15_II	ODT	C3	DQ9
DQ10	U20	SSTL15_II	ODT	C8	DQ10
DQ11	U22	SSTL15_II	ODT	C2	DQ11
DQ12	W20	SSTL15_II	ODT	A7	DQ12
DQ13	W22	SSTL15_II	ODT	A2	DQ13
DQ14	Y21	SSTL15_II	ODT	B8	DQ14
DQ15	Y22	SSTL15_II	ODT	A3	DQ15
LDQS	N20	DIFF_SSTL15_II	ODT	F3	LDQS
LDQS#	N22	DIFF_SSTL15_II	ODT	G3	LDQS#
UDQS	V21	DIFF_SSTL15_II	ODT	C7	UDQS
UDQS#	V22	DIFF_SSTL15_II	ODT	B7	UDQS#
LDM	N19	SSTL15_II	ODT	E7	LDM
UDM	P20	SSTL15_II	ODT	D3	UDM
CK	K20	DIFF_SSTL15_II	100Ω	J7	CK
CK#	L19	DIFF_SSTL15_II		K7	CK#
RZQ	F18	SSTL15_II	100Ω GND	-	-
ZIO	P19	SSTL15_II	open	-	-

Table 4-7 : DDR3 SDRAM Interface

For details regarding the DDR3 SDRAM interface, please refer to the DDR3 SDRAM datasheet and the Xilinx UG388: *Spartan-6 FPGA Memory Controller User Guide*.

4.7.2 SPI-Flash

The TPMC632 provides two Winbond W25Q32 32-Mbit serial Flash memory, one of these Flash can be used as FPGA configuration source. The second serial Flash contains configurable TPMC632 FPGA Example design.

After configuration, it is always accessible from the FPGA, so it also can be used for code or user data storage.

The SPI-EEPROM is connected via Quad (x4) SPI interface to Spartan6 configuration interface.

SPI-PROM Signal	Bank	V_{CCO}	Pin	Description / Spartan6
CLK	2	3.3V	Y20	Serial Clock (CCLK)
CS#	2	3.3V	AA3	Chip Select (CS0_B)
DI (bit0)	2	3.3V	AB20	Serial Data input (MOSI) / MISO[0]
DO (bit1)	2	3.3V	AA20	Serial Data output (DIN) / MISO[1]
WP# (bit2)	2	3.3V	R13	MISO[2]
HOLD# (bit3)	2	3.3V	T14	MISO[3]

Table 4-8 : FPGA SPI-Flash Connections

4.8 User GPIO

The TPMC632 has some general purpose I/O and debug signals connected to FPGA Bank 1. The required signaling standard is LVCMOS15, due to Memory Controller Block usage.

Two pins of the FPGA are routed to the Debug Connector for use as debug interface (UART). This is not a real RS-232 interface. A RS-232 transceiver or USB-UART that can work with 1.5V I/O voltage should be connected to these signals such as TEWS TA900.

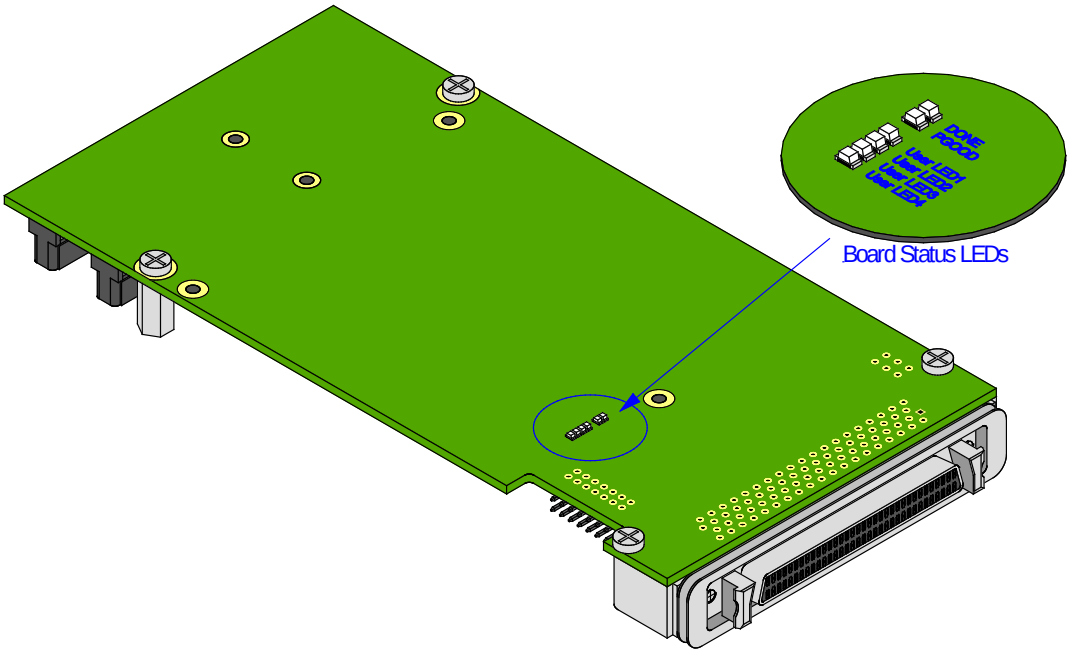
A general purpose I/O Signal is also connected to the Debug Connector. When used with the TEWS TA900, this signal is connected to a Push button and must be configured as FPGA input.

Signal	Bank	V_{CCO}	Pin	Description
GPIO_LED0	1	1.5V	M16	4x green on board LEDs
GPIO_LED1			N15	
GPIO_LED2			U19	
GPIO_LED3			T20	
FPGA_BUT	1	1.5V	D21	General Purpose User I/O
FPGA_RXD	1	1.5V	L15	Serial Debug Interface is accessible via TEWS debug-connector.
FPGA_TXD	1	1.5V	K16	

Table 4-9 : FPGA General Purpose I/O

4.9 On Board Indicators

The TPMC632 provides a couple of board-status LEDs as shown below. These include Power-Good and FPGA configuration status indications as well as four general purpose LEDs.



LED	Color	Description
PGOOD	Green	Power Good Signal for all on board power supplies.
DONE	Red	FPGA DONE-Pin LED Indicates successful FPGA configuration
USER 1 USER 2 USER 3 USER 4	Green Green Green Green	Design dependent, can be controlled by the FPGA. Refer to chapter “User-GPIO”

Table 4-10: Board-Status and User LEDs

4.10 Thermal Management

Power dissipation is design dependent. Main factors are device utilization, frequency and GTP-transceiver usage. Use the Xilinx XPower Estimator (XPE) or XPower Analyzer to determine whether additional cooling requirements as forced air cooling apply. Forced air cooling is recommended during operation.

The TPMC632 has a heat sink mounted on the Spartan-6 FPGA.

5 Design Help

5.1 Example Design

User applications for the TPMC632 can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com.

TEWS offers an FPGA Development Kit (TPMC632-FDK) which consists of well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TPMC632. It implements a DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O functions. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream. This example design can be used as a starting point for own projects.

The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available) or can be licensed separately. It will not work with the free ISE WebPACK.

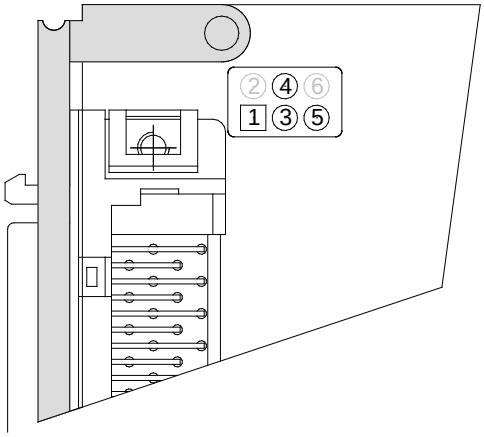
6 Installation

6.1 Pull Up Voltage

The voltage of the pull up resistors can be either 3.3V, 5V or alternatively GND, specified by jumper J1. The default pull up voltage is 5V.

J1 Jumper Position	Pull (Up) Voltage
1 – 3	3.3V
3 – 5	5V (default)
4 – 3	GND

Figure 6-1 : Pull (Up) Voltage Jumper Setting



6.2 I/O Interface

6.2.1 TTL I/O Interface

Each of the 64 (TPMC632x0) or 32 (TPMC632x2) TTL I/O line contains two 74LVT126 bus buffers as an interface to the FPGA pins. The logic levels of the buffers are TTL compatible, meaning that the minimum high level is 2.0V and the maximum low level is 0.8V. The nominal output high voltage is 3.3V.

The buffer outputs are followed by 47Ω serial resistors for signal integrity reasons. The 4.7kΩ pull up resistors guaranty a high level when outputs are tristate and not driven externally.

As an option, the pull up voltage can be set to 5V by jumper J1 to (weakly) drive a higher voltage than 3.3V. This means, instead of toggling the corresponding FPGA_OUT I/O pin, the corresponding FPGA_OE pin (output enable) can be used, to pull the line low or set it in tristate to obtain a high-level. For example when connecting to a standard 5V CMOS logic input (not TTL compatible levels), a high level of minimum 3.5V is required.

Please note that the pull up resistors can only drive high impedance inputs.

A TVS array protects against ESD shocks.

See the following figure for more information of the TTL I/O circuitry.

Please note that the length (and consequently the capacitance) of a flat cable, connected to the TPMC632 module, should be kept as short as possible to prevent large cross talk.

To reduce the cross talk on the TPMC632, not all 64 I/O lines should be switched at the same time. For example, the output lines should be switched in groups of 8 signals in steps of 12ns, meaning that after about 100ns the switching process is completed.

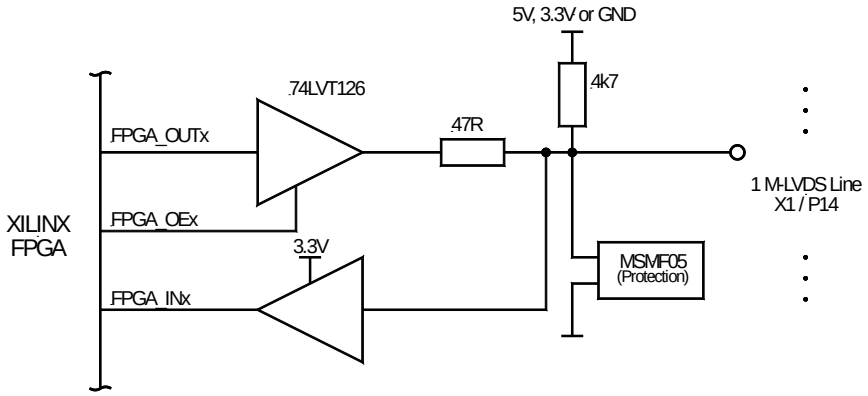


Figure 6-2 : TTL I/O Interface

6.2.2 Differential I/O Interface

Each of the 32 (TPMC632-x1R) or 16 (TPMC632-x2R) differential I/O line pairs is connected on the one side with an input, output and output enable pin at the XILINX FPGA. On the other side connected to a MAX3078E, an ESD-protected RS485/RS422 transceiver and a 120Ω termination resistor.

See the following figure for more information of the differential I/O circuitry.

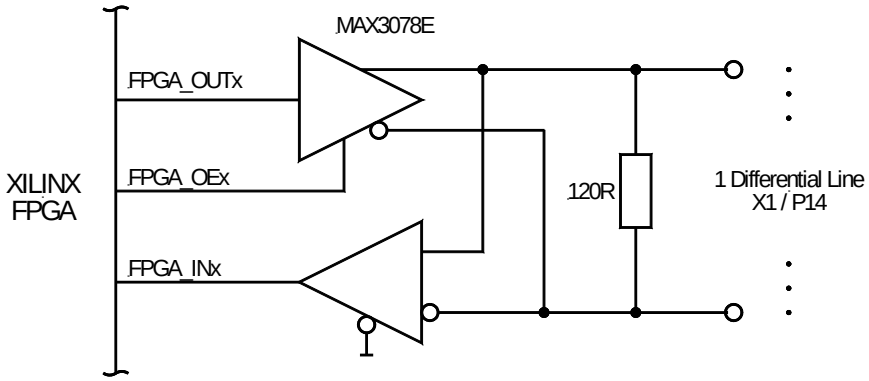


Figure 6-3 : Differential I/O Interface

6.2.3 Multipoint-LVDS Interface

Each of the 32 (TPMC632-x3R) or 16 (TPMC632-x4R) M-LVDS I/O line pairs is connected on the one side with an input, output and output enable pin at the XILINX FPGA and on the other side connected to a M-LVDS transceiver and a 100Ω termination resistor.

See the following figure for more information of the M-LVDS I/O circuitry.

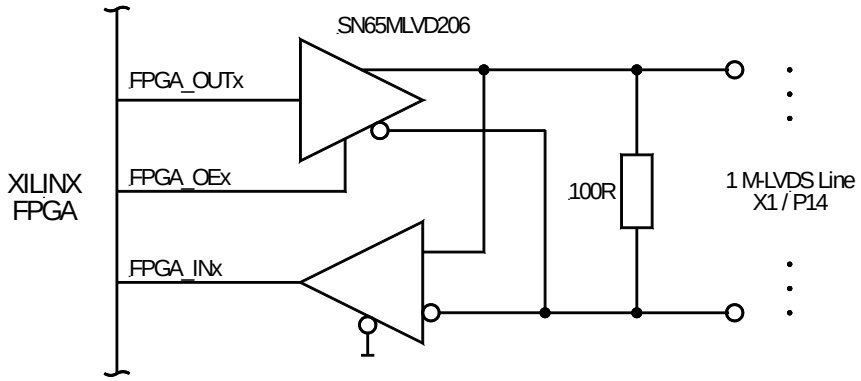


Figure 6-4 : M-LVDS I/O Interface

Please consider that each TPMC632 M-LVDS line has his own termination. If more than four lines are connected together some termination resistors must be removed.

The actual data transmission rate depends on different factors like connection, cable length, fpga design etc.

6.3 Back I/O Configuration

The configuration of P14 64 pin Mezzanine “Back I/O” connector lines [57..64] can be changed to ground instead of IO_56 .. IO_63 signals by change of zero ohm resistors.

The TPMC632 is sensitive to static electricity. Packing, unpacking and all other handling of the TPMC632 has to be done in an ESD/EOS protected Area.

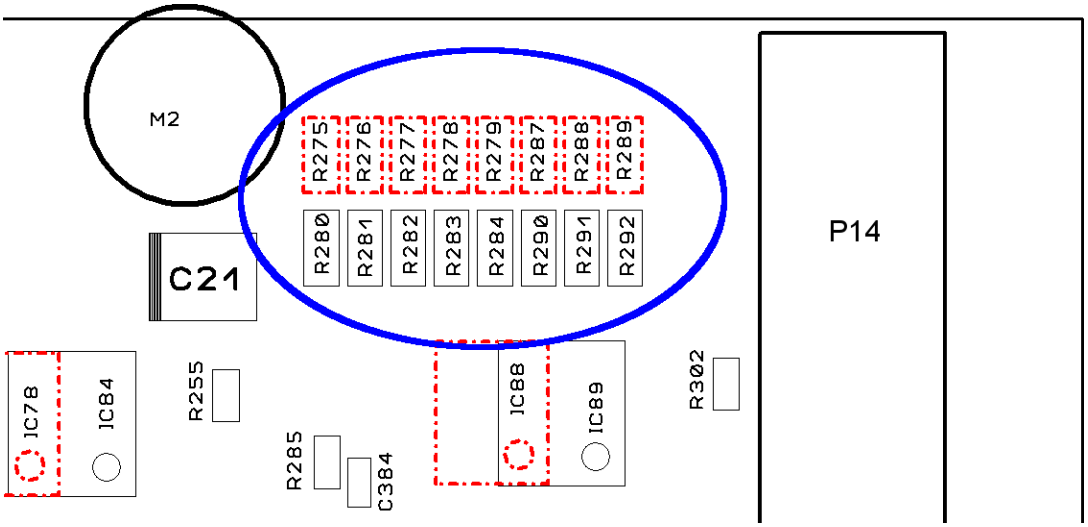


Figure 6-5 : Jumper positions for ground option

Back I/O Line	Signal	Jumper Position
57	ground	R288
	IO_56 / IO_28A/- (default)	R291
58	ground	R289
	I/O_57 / IO_28B/+ (default)	R292
59	ground	R279
	I/O_58 / IO_29A/- (default)	R284
60	ground	R287
	I/O_59 / IO_29B/+ (default)	R290
61	ground	R277
	I/O_60 / IO_30A/- (default)	R282
62	ground	R278
	I/O_61 / IO_30B/+ (default)	R283
63	ground	R275
	I/O_62 / IO_31A/- (default)	R280
64	ground	R276
	I/O_63 / IO_31B/+ (default)	R281

Figure 6-6 : Jumper positions for Back I/O options

Caution: Never make simultaneous connections on both jumper positions of one I/O line. Serious damage of the module is possible.

6.4 FPGA Debug Connector

The Debug Connector (X3) of the TPMC632 can be used to connect a debug adapter, if necessary. The debug adapter must be connected to the TPMC632 prior to PMC-Carrier installation. It is recommended to use the TEWS TA900 Debug Adapter.

The Debug Connector provides three logical interfaces: JTAG, FPGA-UART and one General Purpose User Signal (GPIO_BUT).

- The JTAG interface consists of the signals TDI, TDO, TMS, TCK, uses 3.3V I/O voltage, and can run with up to 6 MHz.
- The FPGA-UART consists of Rx and Tx and uses 1.5V I/O voltage. Communication settings depend on the FPGA programming.
- The General Purpose User Signal uses 1.5V I/O voltage. When used with the TEWS TA900, this signal is connected to a Push button on the TEWS TA900 and must be configured as FPGA input.

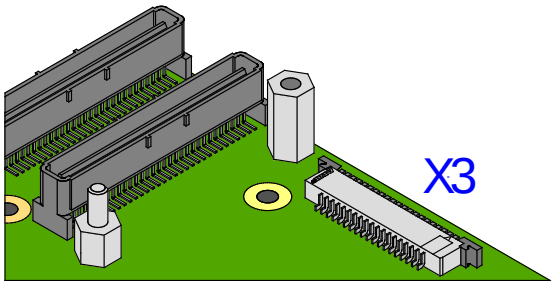
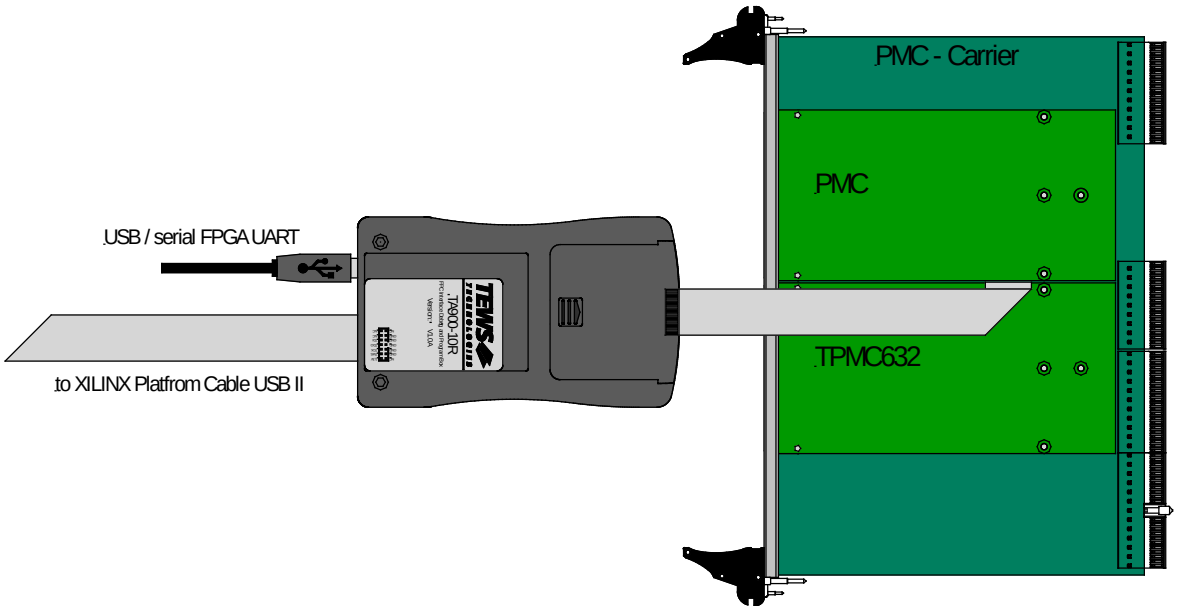


Figure 6-7 : Debug Connector X3

6.4.1 Connecting TA900 to TPMC632 Debug Connector



6.5 FPGA JTAG Connector

The FPGA JTAG connector X2 lets the user directly connect a JTAG interface cable to the on board JTAG chain, e.g. for FPGA read back and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

A through hole, right angle 90° connector with 7 x 2 pins and 2 mm pitch is mounted (Molex 0877601416 or compatible).

With a mounted 2mm pitch flat cable this is of cause a violation of the maximum component height given by the CMC specification, be sure that there is enough space to carrier board.

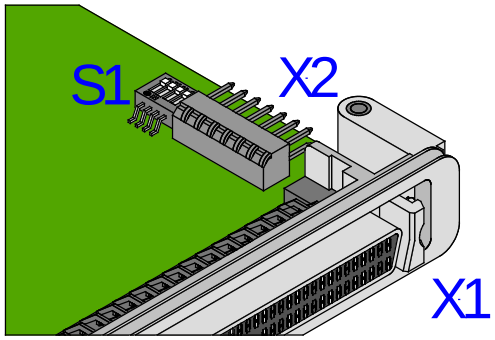
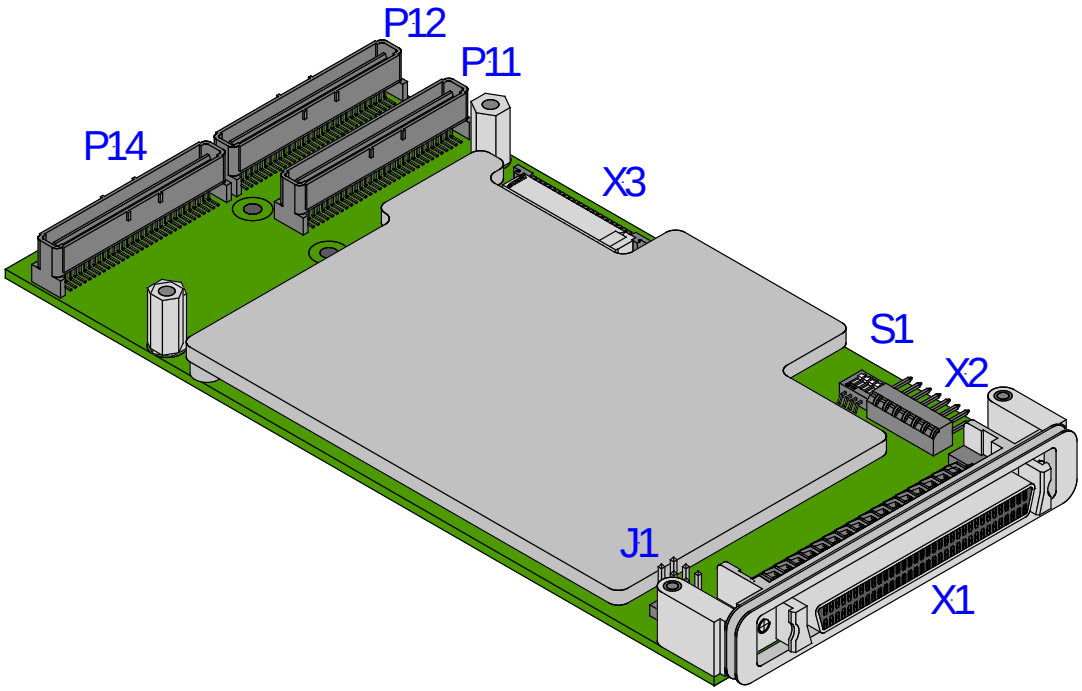


Figure 6-8 : FPGA JTAG Connector X2

7 Pin Assignment – I/O Connector

7.1 Overview



7.2 X1 Front Panel I/O Connector

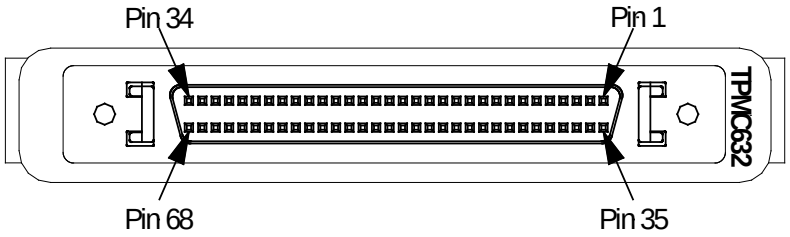


Figure 7-1 : Front Panel I/O Connector Numbering

7.2.1 Connector Type

Pin-Count	68
Connector Type	HD68 SCSI-3 type female connector
Source & Order Info	AMP 787082-7 or compatible

7.2.2 Pin Assignment

Pin	-x0R	-x1R / -x3R	-x2R / -x4R
1	IO_0	IO_0A/-	IO_0A/-
2	IO_2	IO_1A/-	IO_1A/-
3	IO_4	IO_2A/-	IO_2A/-
4	IO_6	IO_3A/-	IO_3A/-
5	IO_8	IO_4A/-	IO_4A/-
6	IO_10	IO_5A/-	IO_5A/-
7	IO_12	IO_6A/-	IO_6A/-
8	IO_14	IO_7A/-	IO_7A/-
9	GND	GND	GND
10	IO_16	IO_8A/-	IO_8A/-
11	IO_18	IO_9A/-	IO_9A/-
12	IO_20	IO_10A/-	IO_10A/-
13	IO_22	IO_11A/-	IO_11A/-
14	IO_24	IO_12A/-	IO_12A/-
15	IO_26	IO_13A/-	IO_13A/-
16	IO_28	IO_14A/-	IO_14A/-
17	IO_30	IO_15A/-	IO_15A/-
18	IO_32	IO_16A/-	IO_32
19	IO_34	IO_17A/-	IO_34
20	IO_36	IO_18A/-	IO_36
21	IO_38	IO_19A/-	IO_38
22	IO_40	IO_20A/-	IO_40
23	IO_42	IO_21A/-	IO_42
24	IO_44	IO_22A/-	IO_44
25	IO_46	IO_23A/-	IO_46
26	GND	GND	GND
27	IO_48	IO_24A/-	IO_48
28	IO_50	IO_25A/-	IO_50
29	IO_52	IO_26A/-	IO_52
30	IO_54	IO_27A/-	IO_54
31	IO_56	IO_28A/-	IO_56
32	IO_58	IO_29A/-	IO_58
33	IO_60	IO_30A/-	IO_60
34	IO_62	IO_31A/-	IO_62

Pin	-x0R	-x1R / -x3R	-x2R / -x4R
35	IO_1	IO_0B/+	IO_0B/+
36	IO_3	IO_1B/+	IO_1B/+
37	IO_5	IO_2B/+	IO_2B/+
38	IO_7	IO_3B/+	IO_3B/+
39	IO_9	IO_4B/+	IO_4B/+
40	IO_11	IO5B/+	IO5B/+
41	IO_13	IO6B/+	IO6B/+
42	IO_15	IO_7B/+	IO_7B/+
43	GND	GND	GND
44	IO_17	IO_8B/+	IO_8B/+
45	IO_19	IO_9B/+	IO_9B/+
46	IO_21	IO_10B/+	IO_10B/+
47	IO_23	IO_11B/+	IO_11B/+
48	IO_25	IO_12B/+	IO_12B/+
49	IO_27	IO_13B/+	IO_13B/+
50	IO_29	IO_14B/+	IO_14B/+
51	IO_31	IO_15B/+	IO_15B/+
52	IO_33	IO_16B/+	IO_33
53	IO_35	IO_17B/+	IO_35
54	IO_37	IO_18B/+	IO_37
55	IO_39	IO_19B/+	IO_39
56	IO_41	IO_20B/+	IO_41
57	IO_43	IO_21B/+	IO_43
58	IO_45	IO_22B/+	IO_45
59	IO_47	IO_23B/+	IO_47
60	GND	GND	GND
61	IO_49	IO_24B/+	IO_49
62	IO_51	IO_25B/+	IO_51
63	IO_53	IO_26B/+	IO_53
64	IO_55	IO_27B/+	IO_55
65	IO_57	IO_28B/+	IO_57
66	IO_59	IO_29B/+	IO_59
67	IO_61	IO_30B/+	IO_61
68	IO_63	IO_31B/+	IO_63

Table 7-1 : Pin Assignment Front Panel I/O Connector X1

7.3 Back I/O PMC Connector P14

7.3.1 Connector Type

Pin-Count	64
Connector Type	64 pol. Mezzanine SMD Connector
Source & Order Info	Molex – 71436-2864 or compatible

7.3.2 Pin Assignment

Pin	-x0R	-x1R / -x3R	-x2R / -x4R
1	IO_0	IO_0A/-	IO_0A/-
2	IO_1	IO_0B/+	IO_0B/+
3	IO_2	IO_1A/-	IO_1A/-
4	IO_3	IO_1B/+	IO_1B/+
5	IO_4	IO_2A/-	IO_2A/-
6	IO_5	IO_2B/+	IO_2B/+
7	IO_6	IO_3A/-	IO_3A/-
8	IO_7	IO_3B/+	IO_3B/+
9	IO_8	IO_4A/-	IO_4A/-
10	IO_9	IO_4B/+	IO_4B/+
11	IO_10	IO_5A/-	IO_5A/-
12	IO_11	IO_5B/+	IO_5B/+
13	IO_12	IO_6A/-	IO_6A/-
14	IO_13	IO_6B/+	IO_6B/+
15	IO_14	IO_7A/-	IO_7A/-
16	IO_15	IO_7B/+	IO_7B/+
17	IO_16	IO_8A/-	IO_8A/-
18	IO_17	IO_8B/+	IO_8B/+
19	IO_18	IO_9A/-	IO_9A/-
20	IO_19	IO_9B/+	IO_9B/+
21	IO_20	IO_10A/-	IO_10A/-
22	IO_21	IO_10B/+	IO_10B/+
23	IO_22	IO_11A/-	IO_11A/-
24	IO_23	IO_11B/+	IO_11B/+
25	IO_24	IO_12A/-	IO_12A/-
26	IO_25	IO_12B/+	IO_12B/+
27	IO_26	IO_13A/-	IO_13A/-
28	IO_27	IO_13B/+	IO_13B/+
29	IO_28	IO_14A/-	IO_14A/-

Pin	-x0R	-x1R / -x3R	-x2R / -x4R
33	IO_32	IO_16A/-	IO_32
34	IO_33	IO_16B/+	IO_33
35	IO_34	IO_17A/-	IO_34
36	IO_35	IO_17B/+	IO_35
37	IO_36	IO_18A/-	IO_36
38	IO_37	IO_18B/+	IO_37
39	IO_38	IO_19A/-	IO_38
40	IO_39	IO_19B/+	IO_39
41	IO_40	IO_20A/-	IO_40
42	IO_41	IO_20B/+	IO_41
43	IO_42	IO_21A/-	IO_42
44	IO_43	IO_21B/+	IO_43
45	IO_44	IO_22A/-	IO_44
46	IO_45	IO_22B/+	IO_45
47	IO_46	IO_23A/-	IO_46
48	IO_47	IO_23B/+	IO_47
49	IO_48	IO_24A/-	IO_48
50	IO_49	IO_24B/+	IO_49
51	IO_50	IO_25A/-	IO_50
52	IO_51	IO_25B/+	IO_51
53	IO_52	IO_26A/-	IO_52
54	IO_53	IO_26B/+	IO_53
55	IO_54	IO_27A/-	IO_54
56	IO_55	IO_27B/+	IO_55
57	IO_56	IO_28A/-	IO_56
58	IO_57	IO_28B/+	IO_57
59	IO_58	IO_29A/-	IO_58
60	IO_59	IO_29B/+	IO_59
61	IO_60	IO_30A/-	IO_60

Pin	-x0R	-x1R / -x3R	-x2R / -x4R
30	IO_29	IO_14B/+	IO_14B/+
31	IO_30	IO_15A/-	IO_15A/-
32	IO_31	IO_15B/+	IO_15B/+

Pin	-x0R	-x1R / -x3R	-x2R / -x4R
62	IO_61	IO_30B/+	IO_61
63	IO_62	IO_31A/-	IO_62
64	IO_63	IO_31B/+	IO_63

Table 7-2 : Pin Assignment Back I/O PMC Connector P14

7.4 X2 JTAG Header

This header directly connects a JTAG interface cable to the JTAG pins to the on board JTAG chain. The pinout of this header matches the pinout of the Xilinx Platform Cable USB II. This allows the direct usage of Xilinx software-tools like Chipscope or iMPACT with the Platform Cable USB II. The connector is a 2 mm dual row shrouded header.

7.4.1 Connector Type

Pin-Count	14
Connector Type	2.00 mm Pitch Milli-Grid™ Header
Source & Order Info	Molex 877601416 or compatible

7.4.2 Pin Assignment

Pin	Signal	Description
1	NC	Not Connected
2	V_{REF}	JTAG Reference Voltage (3.3V)
3	GND	Ground
4	TMS	Test Mode Select Input
5	GND	Ground
6	TCK	Test Clock
7	GND	Ground
8	TDO	Test Data Output (TAP Controller: TDI)
9	GND	Ground
10	TDI	Test Data Input (TAP Controller: TDO)
11	GND	not connected on the TPMC632
12	TRST#	not connected on the TPMC632
13	PGND	Used on TPMC632 for XILINX Header present detection
14	NC	HALT_INIT_WP signal. Optional. Not connected on the TPMC632

Table 7-3 : Pin Assignment JTAG Header X2

7.5 X3 Debug-Connector

7.5.1 Connector Type

Pin-Count	20
Connector Type	20-pin, 1 mm FPC (Flexible Printed Circuit) Connector
Source & Order Info	AMP 2-487951-0 / 2-84953-0 or Molex 0522072060

7.5.2 Pin Assignment

Pin	Signal	I/O	Description
1	JTAG SEL	O	A 4.7k pullup to 3.3 Volt is located on the TPMC632
2	3.3V	O	JTAG reference I/O voltage
3	TDO	O	Test Data Output (Input at JTAG Interface)
4	GND	-	Ground
5	TDI	I	Test Data Input (Output at JTAG Interface)
6	TMS	I	Test Mode Select Input
7	GND	-	Ground
8	TCK	I	Test Clock
9	GND	-	Ground
10	UART_RxD	I	FPGA UART Receive Data (Input)
11	1.5V	O	UART reference I/O voltage
12	UART_TxD	O	FPGA UART Transmit Data (Output)
13	GND	-	Ground
14	NC	-	Not used on TPMC632
15	NC	-	Not used on TPMC632
16	NC	-	Not used on TPMC632
17	GND	-	Ground
18	3.3V	O	+3.3 Volt
19	1.5V	O	User signal reference I/O voltage
20	GPIO_BUT	I	User signal connected to the FPGA, A 4.7k pullup to 1.5 Volt is located on the TPMC632

Table 7-4 : Pin Assignment Debug Connector X3

8 Known Issues

Level Switching at TPMC632 I/O Lines during FPGA Configuration.

At power-up or after a FPGA reconfiguration is started, the FPGA need up to 10ms to start configuration. During this time, the I/O lines of the TPMC632 may randomly toggle between high and low in case that I/O Line 19 of the TPMC632 (X1 pin 45 resp. P14 pin 20) is low.

As long as the TPMC632 is used with J1 configured as a Pull-up and I/O Line 19 is not connected to GND or driven low externally, this issue does not occur.

To avoid this issue, the TPMC632-xxR I/O Line 19 should have a minimum of +2V DC (lower limit of TTL high level) during FPGA configuration.

9 Appendix A

This appendix contains the signal to pin assignments for the Spartan6 FPGA.

```
## ############################################################################################################ ##
##                                          TEWS TECHNOLOGIES                                                   ##
## ############################################################################################################ ##
##
##   Project Name    : TPMC632-xx_FPGA
##   File Name               : tpmc632-xx_fpga.ucf
##   Target Device   : XC6SLXxxT-xFGG484
##   Design Tool     : Xilinx ISE Design Suit Embedded 13.3
##   Simulation Tool : Xilinx ISIM included in Design Tool
##
##   Description     : The file lists all FPGA pins that are connected on the TPMC632
##
##   Owner           : TEWS TECHNOLOGIES GmbH
##                     Am Bahnhof 7
##                     D-25469 Halstenbek
##
##                     Tel.: +49 / (0)4101 / 4058-0
##                     Fax.: +49 / (0)4101 / 4058-19
##                     e-mail: support@tews.com
##
##                     Copyright (c) 2011
##                     TEWS TECHNOLOGIES GmbH
##
##   History         :
##       Version   1 : (SE, 23.06.2011)
##                     Initial Version
##       Version   2 : (SE, 31.08.2011)
##                     The following changes occur in the new version:
##                     - Fixed GPIO LED location constraints
##                     - Corrected constraints for FPGA_IN[29], FPGA_IN[30] and FPGA_OUT[25]
##       Version   3 : (SE, 25.10.2011)
##                     Adapted pin locations to post layout results
##       Version   4 : (SE, 02.12.2011)
##                     File Rename / Revised Header
##       Version   5 : (SE, 13.12.2011)
##                     Added driver strength and slew rate on I/O lines for improved signal
integrity
##       Version   6 : (SE, 11.01.2012)
##                     Updated pin-bank affiliation comment for FPGA_OE and FPGA_OUT pins
##
##   Comments        : none
##
## ############################################################################################################ ##


## ############################################################################################################ ##
## Section: Miscellaneous
## ############################################################################################################ ##

# Set VCC aux power supply values (necessary for Spartan-6 architecture)
config vccaux = 3.3;


# Prohibit usage of pins that are not allowed for user I/O
config prohibit                          = "Y20";          # CCLK Bank 2

config prohibit                          = "AA21";         # M0 Bank 2
config prohibit                          = "Y19";          # M1 Bank 2

# For data pins D0, D1 and D2 refer section SPI
config prohibit                          = "AA6";          # D3 Bank 2
config prohibit                          = "AB6";          # D4 Bank 2
config prohibit                          = "Y5";           # D5 Bank 2
config prohibit                          = "AB5";          # D6 Bank 2
config prohibit                          = "W9";           # D7 Bank 2

config prohibit                          = "Y8";           # RDWR_B Bank 2
```

```
config prohibit                          = "Y4";          # INIT_B Bank 2
config prohibit                          = "AA3";         # CSO_B Bank 2
config prohibit                          = "AB2";         # PROGRAM_B Bank 2

config prohibit                          = "AA12";        # D14 Bank 2


## ############################################################################################## ##
## Section: SPI
## ############################################################################################## ##

# Define I/O Standard
net "MISO[*]"                  iostandard = LVCMOS33;      # Bank 2 Supply 3.3V


# Define Location Constraints
net "MISO[0]"                            loc = "AB20";     # Bank 2, MOSI
net "MISO[1]"                            loc = "AA20";     # Bank 2, D0
net "MISO[2]"                            loc = "R13";      # Bank 2, D1
net "MISO[3]"                            loc = "T14";      # Bank 2, D2


## ############################################################################################## ##
## Section: PCI Express
## ############################################################################################## ##

# Define Location Constraints
net "PCIe_TX_C_P"                        loc = "B6";       # Bank 101
net "PCIe_TX_C_N"                        loc = "A6";       # Bank 101
net "PCIe_RX_C_P"                        loc = "D7";       # Bank 101
net "PCIe_RX_C_N"                        loc = "C7";       # Bank 101

net "PCIe_REFCLK_P"                      loc = "A10";      # Bank 101
net "PCIe_REFCLK_N"                      loc = "B10";      # Bank 101


## ############################################################################################## ##
## Section: TTL I/O
## ############################################################################################## ##

# Define I/O Standard
net "FPGA_OE[*]"               iostandard = LVCMOS33;      # Bank 0/2/3 Supply 3.3V
net "FPGA_IN[*]"               iostandard = LVCMOS33;      # Bank 0/2/3 Supply 3.3V
net "FPGA_OUT[*]"              iostandard = LVCMOS33;      # Bank 2/3   Supply 3.3V


# I/O Standard Enhancement
net "FPGA_OE[*]"               slow | drive = 8;           # Settings for Signal Integrity
net "FPGA_OUT[*]"              slow | drive = 8;           # Settings for Signal Integrity


# Define Location Constraints
net "FPGA_OE[0]"                         loc = "T15";      # Bank 2
net "FPGA_OE[1]"                         loc = "AB16";     # Bank 2
net "FPGA_OE[2]"                         loc = "AB11";     # Bank 2
net "FPGA_OE[3]"                         loc = "AB8";      # Bank 2
net "FPGA_OE[4]"                         loc = "AB10";     # Bank 2
net "FPGA_OE[5]"                         loc = "AB7";      # Bank 2
net "FPGA_OE[6]"                         loc = "W8";       # Bank 2
net "FPGA_OE[7]"                         loc = "AB9";      # Bank 2
net "FPGA_OE[8]"                         loc = "R8";       # Bank 2
net "FPGA_OE[9]"                         loc = "AB4";      # Bank 2
net "FPGA_OE[10]"                        loc = "AB17";     # Bank 2
net "FPGA_OE[11]"                        loc = "AB15";     # Bank 2
net "FPGA_OE[12]"                        loc = "W12";      # Bank 2

net "FPGA_OE[13]"                        loc = "R1";       # Bank 3
net "FPGA_OE[14]"                        loc = "V1";       # Bank 3

net "FPGA_OE[15]"                        loc = "T7";       # Bank 2
net "FPGA_OE[16]"                        loc = "U6";       # Bank 2
net "FPGA_OE[17]"                        loc = "AB19";     # Bank 2
```

```
net "FPGA_OE[18]"                   loc = "C1";          # Bank 3
net "FPGA_OE[19]"                   loc = "M8";          # Bank 3

net "FPGA_OE[20]"                   loc = "AA18";        # Bank 2
net "FPGA_OE[21]"                   loc = "AB18";        # Bank 2
net "FPGA_OE[22]"                   loc = "U14";         # Bank 2
net "FPGA_OE[23]"                   loc = "W14";         # Bank 2
net "FPGA_OE[24]"                   loc = "Y16";         # Bank 2
net "FPGA_OE[25]"                   loc = "U16";         # Bank 2
net "FPGA_OE[26]"                   loc = "V13";         # Bank 2
net "FPGA_OE[27]"                   loc = "W13";         # Bank 2

net "FPGA_OE[28]"                   loc = "U1";          # Bank 3
net "FPGA_OE[29]"                   loc = "AA1";         # Bank 3

net "FPGA_OE[30]"                   loc = "U13";         # Bank 2

net "FPGA_OE[31]"                   loc = "AA2";         # Bank 3

net "FPGA_OE[32]"                   loc = "W6";          # Bank 2

net "FPGA_OE[33]"                   loc = "W4";          # Bank 3
net "FPGA_OE[34]"                   loc = "R3";          # Bank 3
net "FPGA_OE[35]"                   loc = "T6";          # Bank 3
net "FPGA_OE[36]"                   loc = "D1";          # Bank 3
net "FPGA_OE[37]"                   loc = "V3";          # Bank 3
net "FPGA_OE[38]"                   loc = "H5";          # Bank 3
net "FPGA_OE[39]"                   loc = "J6";          # Bank 3
net "FPGA_OE[40]"                   loc = "F2";          # Bank 3
net "FPGA_OE[41]"                   loc = "G1";          # Bank 3
net "FPGA_OE[42]"                   loc = "H2";          # Bank 3
net "FPGA_OE[43]"                   loc = "H1";          # Bank 3
net "FPGA_OE[44]"                   loc = "U3";          # Bank 3
net "FPGA_OE[45]"                   loc = "U4";          # Bank 3
net "FPGA_OE[46]"                   loc = "T3";          # Bank 3
net "FPGA_OE[47]"                   loc = "P6";          # Bank 3
net "FPGA_OE[48]"                   loc = "R7";          # Bank 3
net "FPGA_OE[49]"                   loc = "M7";          # Bank 3

net "FPGA_OE[50]"                   loc = "U8";          # Bank 2

net "FPGA_OE[51]"                   loc = "M2";          # Bank 3
net "FPGA_OE[52]"                   loc = "T4";          # Bank 3
net "FPGA_OE[53]"                   loc = "V5";          # Bank 3
net "FPGA_OE[54]"                   loc = "K1";          # Bank 3
net "FPGA_OE[55]"                   loc = "N1";          # Bank 3
net "FPGA_OE[56]"                   loc = "P5";          # Bank 3
net "FPGA_OE[57]"                   loc = "N6";          # Bank 3
net "FPGA_OE[58]"                   loc = "K2";          # Bank 3
net "FPGA_OE[59]"                   loc = "N7";          # Bank 3
net "FPGA_OE[60]"                   loc = "P7";          # Bank 3
net "FPGA_OE[61]"                   loc = "P1";          # Bank 3
net "FPGA_OE[62]"                   loc = "K5";          # Bank 3
net "FPGA_OE[63]"                   loc = "J4";          # Bank 3


net "FPGA_IN[0]"                    loc = "L4";          # Bank 3
net "FPGA_IN[1]"                    loc = "M3";          # Bank 3
net "FPGA_IN[2]"                    loc = "M4";          # Bank 3
net "FPGA_IN[3]"                    loc = "M5";          # Bank 3
net "FPGA_IN[4]"                    loc = "N4";          # Bank 3
net "FPGA_IN[5]"                    loc = "P3";          # Bank 3
net "FPGA_IN[6]"                    loc = "L1";          # Bank 3
net "FPGA_IN[7]"                    loc = "L3";          # Bank 3

net "FPGA_IN[8]"                    loc = "V17";         # Bank 2
net "FPGA_IN[9]"                    loc = "W18";         # Bank 2
net "FPGA_IN[10]"                   loc = "Y17";         # Bank 2
net "FPGA_IN[11]"                   loc = "V15";         # Bank 2
net "FPGA_IN[12]"                   loc = "W17";         # Bank 2
net "FPGA_IN[13]"                   loc = "Y18";         # Bank 2

net "FPGA_IN[14]"                   loc = "V2";          # Bank 3
```

```
net "FPGA_IN[15]"                   loc = "Y1";          # Bank 3

net "FPGA_IN[16]"                   loc = "Y14";         # Bank 2
net "FPGA_IN[17]"                   loc = "Y15";         # Bank 2

net "FPGA_IN[18]"                   loc = "B2";          # Bank 0
net "FPGA_IN[19]"                   loc = "C3";          # Bank 0
net "FPGA_IN[20]"                   loc = "A4";          # Bank 0
net "FPGA_IN[21]"                   loc = "D4";          # Bank 0
net "FPGA_IN[22]"                   loc = "H14";         # Bank 0
net "FPGA_IN[23]"                   loc = "D5";          # Bank 0
net "FPGA_IN[24]"                   loc = "E5";          # Bank 0
net "FPGA_IN[25]"                   loc = "E6";          # Bank 0
net "FPGA_IN[26]"                   loc = "A19";         # Bank 0
net "FPGA_IN[27]"                   loc = "F16";         # Bank 0
net "FPGA_IN[28]"                   loc = "A2";          # Bank 0
net "FPGA_IN[29]"                   loc = "D3";          # Bank 0
net "FPGA_IN[30]"                   loc = "B20";         # Bank 0
net "FPGA_IN[31]"                   loc = "F8";          # Bank 0
net "FPGA_IN[32]"                   loc = "H11";         # Bank 0
net "FPGA_IN[33]"                   loc = "H10";         # Bank 0
net "FPGA_IN[34]"                   loc = "G9";          # Bank 0
net "FPGA_IN[35]"                   loc = "G8";          # Bank 0
net "FPGA_IN[36]"                   loc = "B3";          # Bank 0
net "FPGA_IN[37]"                   loc = "A3";          # Bank 0
net "FPGA_IN[38]"                   loc = "A18";         # Bank 0
net "FPGA_IN[39]"                   loc = "B18";         # Bank 0
net "FPGA_IN[40]"                   loc = "A17";         # Bank 0
net "FPGA_IN[41]"                   loc = "A5";          # Bank 0
net "FPGA_IN[42]"                   loc = "C5";          # Bank 0
net "FPGA_IN[43]"                   loc = "C4";          # Bank 0
net "FPGA_IN[44]"                   loc = "G13";         # Bank 0
net "FPGA_IN[45]"                   loc = "G15";         # Bank 0
net "FPGA_IN[46]"                   loc = "D17";         # Bank 0
net "FPGA_IN[47]"                   loc = "E16";         # Bank 0
net "FPGA_IN[48]"                   loc = "G16";         # Bank 0
net "FPGA_IN[49]"                   loc = "F17";         # Bank 0
net "FPGA_IN[50]"                   loc = "D18";         # Bank 0
net "FPGA_IN[51]"                   loc = "D19";         # Bank 0
net "FPGA_IN[52]"                   loc = "F15";         # Bank 0
net "FPGA_IN[53]"                   loc = "F9";          # Bank 0
net "FPGA_IN[54]"                   loc = "C19";         # Bank 0
net "FPGA_IN[55]"                   loc = "F7";          # Bank 0
net "FPGA_IN[56]"                   loc = "G11";         # Bank 0
net "FPGA_IN[57]"                   loc = "F14";         # Bank 0
net "FPGA_IN[58]"                   loc = "C18";         # Bank 0
net "FPGA_IN[59]"                   loc = "C17";         # Bank 0
net "FPGA_IN[60]"                   loc = "A20";         # Bank 0
net "FPGA_IN[61]"                   loc = "H12";         # Bank 0
net "FPGA_IN[62]"                   loc = "F10";         # Bank 0
net "FPGA_IN[63]"                   loc = "H13";         # Bank 0


net "FPGA_OUT[0]"                   loc = "Y3";          # Bank 3

net "FPGA_OUT[1]"                   loc = "AB14";        # Bank 2
net "FPGA_OUT[2]"                   loc = "AB12";        # Bank 2
net "FPGA_OUT[3]"                   loc = "AA4";         # Bank 2

net "FPGA_OUT[4]"                   loc = "N3";          # Bank 3
net "FPGA_OUT[5]"                   loc = "W3";          # Bank 3

net "FPGA_OUT[6]"                   loc = "AA10";        # Bank 2
net "FPGA_OUT[7]"                   loc = "Y6";          # Bank 2

net "FPGA_OUT[8]"                   loc = "M6";          # Bank 3
net "FPGA_OUT[9]"                   loc = "L6";          # Bank 3
net "FPGA_OUT[10]"                  loc = "K4";          # Bank 3
net "FPGA_OUT[11]"                  loc = "K3";          # Bank 3
net "FPGA_OUT[12]"                  loc = "P2";          # Bank 3
net "FPGA_OUT[13]"                  loc = "T1";          # Bank 3
net "FPGA_OUT[14]"                  loc = "J3";          # Bank 3
net "FPGA_OUT[15]"                  loc = "R4";          # Bank 3
```

```
net "FPGA_OUT[16]"                    loc = "T5";          # Bank 3
net "FPGA_OUT[17]"                    loc = "M1";          # Bank 3
net "FPGA_OUT[18]"                    loc = "D2";          # Bank 3
net "FPGA_OUT[19]"                    loc = "J7";          # Bank 3
net "FPGA_OUT[20]"                    loc = "F1";          # Bank 3
net "FPGA_OUT[21]"                    loc = "H3";          # Bank 3
net "FPGA_OUT[22]"                    loc = "G3";          # Bank 3

net "FPGA_OUT[23]"                    loc = "Y9";          # Bank 2
net "FPGA_OUT[24]"                    loc = "Y12";         # Bank 2

net "FPGA_OUT[25]"                    loc = "T2";          # Bank 3
net "FPGA_OUT[26]"                    loc = "E3";          # Bank 3

net "FPGA_OUT[27]"                    loc = "AA16";        # Bank 2

net "FPGA_OUT[28]"                    loc = "Y2";          # Bank 3
net "FPGA_OUT[29]"                    loc = "W1";          # Bank 3
net "FPGA_OUT[30]"                    loc = "K7";          # Bank 3
net "FPGA_OUT[31]"                    loc = "K8";          # Bank 3
net "FPGA_OUT[32]"                    loc = "H4";          # Bank 3
net "FPGA_OUT[33]"                    loc = "G4";          # Bank 3

net "FPGA_OUT[34]"                    loc = "AA8";         # Bank 2
net "FPGA_OUT[35]"                    loc = "V7";          # Bank 2

net "FPGA_OUT[36]"                    loc = "F3";          # Bank 3
net "FPGA_OUT[37]"                    loc = "E4";          # Bank 3
net "FPGA_OUT[38]"                    loc = "H6";          # Bank 3
net "FPGA_OUT[39]"                    loc = "G7";          # Bank 3
net "FPGA_OUT[40]"                    loc = "E1";          # Bank 3
net "FPGA_OUT[41]"                    loc = "H8";          # Bank 3
net "FPGA_OUT[42]"                    loc = "F5";          # Bank 3
net "FPGA_OUT[43]"                    loc = "G6";          # Bank 3
net "FPGA_OUT[44]"                    loc = "B1";          # Bank 3

net "FPGA_OUT[45]"                    loc = "W15";         # Bank 2

net "FPGA_OUT[46]"                    loc = "K6";          # Bank 3
net "FPGA_OUT[47]"                    loc = "P8";          # Bank 3

net "FPGA_OUT[48]"                    loc = "R9";          # Bank 2
net "FPGA_OUT[49]"                    loc = "V11";         # Bank 2
net "FPGA_OUT[50]"                    loc = "Y10";         # Bank 2

net "FPGA_OUT[51]"                    loc = "P4";          # Bank 3

net "FPGA_OUT[52]"                    loc = "V9";          # Bank 2
net "FPGA_OUT[53]"                    loc = "W10";         # Bank 2
net "FPGA_OUT[54]"                    loc = "W11";         # Bank 2
net "FPGA_OUT[55]"                    loc = "U9";          # Bank 2
net "FPGA_OUT[56]"                    loc = "T8";          # Bank 2
net "FPGA_OUT[57]"                    loc = "T10";         # Bank 2
net "FPGA_OUT[58]"                    loc = "U10";         # Bank 2
net "FPGA_OUT[59]"                    loc = "Y7";          # Bank 2

net "FPGA_OUT[60]"                    loc = "J1";          # Bank 3

net "FPGA_OUT[61]"                    loc = "U15";         # Bank 2
net "FPGA_OUT[62]"                    loc = "R11";         # Bank 2
net "FPGA_OUT[63]"                    loc = "T11";         # Bank 2


## ##############################################################################################
## Section: DDR3 Memory
## ##############################################################################################

# MCB 3, I/O Termination
net "DDR_DQ[*]"                    in_term = none;
net "DDR_?DQS_?"                   in_term = none;

# MCB 3, I/O Standards
net "DDR_DQ[*]"                iostandard = SSTL15_II;      # 1.5V
```

```
net "DDR_A[*]"                iostandard = SSTL15_II;      # 1.5V
net "DDR_BA[*]"               iostandard = SSTL15_II;      # 1.5V
net "DDR_?DQS_?"              iostandard = DIFF_SSTL15_II; # 1.5V
net "DDR_CK_?"                iostandard = DIFF_SSTL15_II; # 1.5V
net "DDR_CKe"                 iostandard = SSTL15_II;      # 1.5V
net "DDR_RAS_n"               iostandard = SSTL15_II;      # 1.5V
net "DDR_CAS_n"               iostandard = SSTL15_II;      # 1.5V
net "DDR_WE_n"                iostandard = SSTL15_II;      # 1.5V
net "DDR_ODT"                 iostandard = SSTL15_II;      # 1.5V
net "DDR_RESET_n"             iostandard = LVCMOS15;       # 1.5V
net "DDR_?DM"                 iostandard = SSTL15_II;      # 1.5V
net "DDR_RZQ"                 iostandard = SSTL15_II;      # 1.5V
net "DDR_ZIO"                 iostandard = SSTL15_II;      # 1.5V


# MCB 3, Pin Location Constraints for Clock, Masks, Address, and Controls
net "DDR_A[0]"                          loc = "H21";          # Bank 1
net "DDR_A[1]"                          loc = "H22";          # Bank 1
net "DDR_A[2]"                          loc = "G22";          # Bank 1
net "DDR_A[3]"                          loc = "J20";          # Bank 1
net "DDR_A[4]"                          loc = "H20";          # Bank 1
net "DDR_A[5]"                          loc = "M20";          # Bank 1
net "DDR_A[6]"                          loc = "M19";          # Bank 1
net "DDR_A[7]"                          loc = "G20";          # Bank 1
net "DDR_A[8]"                          loc = "E20";          # Bank 1
net "DDR_A[9]"                          loc = "E22";          # Bank 1
net "DDR_A[10]"                         loc = "J19";          # Bank 1
net "DDR_A[11]"                         loc = "H19";          # Bank 1
net "DDR_A[12]"                         loc = "F22";          # Bank 1
net "DDR_A[13]"                         loc = "G19";          # Bank 1
net "DDR_A[14]"                         loc = "F20";          # Bank 1

net "DDR_BA[0]"                         loc = "K17";          # Bank 1
net "DDR_BA[1]"                         loc = "L17";          # Bank 1
net "DDR_BA[2]"                         loc = "K18";          # Bank 1

net "DDR_CK_P"                          loc = "K20";          # Bank 1
net "DDR_CK_N"                          loc = "L19";          # Bank 1

net "DDR_DQ[0]"                         loc = "R20";          # Bank 1
net "DDR_DQ[1]"                         loc = "R22";          # Bank 1
net "DDR_DQ[2]"                         loc = "P21";          # Bank 1
net "DDR_DQ[3]"                         loc = "P22";          # Bank 1
net "DDR_DQ[4]"                         loc = "L20";          # Bank 1
net "DDR_DQ[5]"                         loc = "L22";          # Bank 1
net "DDR_DQ[6]"                         loc = "M21";          # Bank 1
net "DDR_DQ[7]"                         loc = "M22";          # Bank 1
net "DDR_DQ[8]"                         loc = "T21";          # Bank 1
net "DDR_DQ[9]"                         loc = "T22";          # Bank 1
net "DDR_DQ[10]"                        loc = "U20";          # Bank 1
net "DDR_DQ[11]"                        loc = "U22";          # Bank 1
net "DDR_DQ[12]"                        loc = "W20";          # Bank 1
net "DDR_DQ[13]"                        loc = "W22";          # Bank 1
net "DDR_DQ[14]"                        loc = "Y21";          # Bank 1
net "DDR_DQ[15]"                        loc = "Y22";          # Bank 1

net "DDR_CKE"                           loc = "F21";          # Bank 1
net "DDR_ODT"                           loc = "J22";          # Bank 1

net "DDR_LDQS_P"                        loc = "N20";          # Bank 1
net "DDR_LDQS_N"                        loc = "N22";          # Bank 1
net "DDR_UDQS_P"                        loc = "V21";          # Bank 1
net "DDR_UDQS_N"                        loc = "V22";          # Bank 1

net "DDR_CAS_n"                         loc = "K22";          # Bank 1
net "DDR_RAS_n"                         loc = "K21";          # Bank 1
net "DDR_WE_n"                          loc = "K19";          # Bank 1

net "DDR_LDM"                           loc = "N19";          # Bank 1
net "DDR_UDM"                           loc = "P20";          # Bank 1

net "DDR_RESET_n"                       loc = "H18";          # Bank 1
```

```
net "DDR_RZQ"                           loc = "F18";          # Bank 1
net "DDR_ZIO"                           loc = "P19";          # Bank 1


# Additional Constratints
config mcb_performance                      = standard;       # General MCB constraints


## ##############################################################################################
## Section: Clocking
## ##############################################################################################

# Define I/O Standards
net "CLKGEN_S*"                 iostandard = LVCMOS15;       # Bank 1 Supply 1.5V
net "CLKGEN_INTR"               iostandard = LVCMOS15;       # Bank 1 Supply 1.5V

net "USER_CCLK"                 iostandard = LVCMOS33;       # Bank 2 Supply 3.3V
net "MCB_CLK"                   iostandard = LVCMOS33;       # Bank 2 Supply 3.3V
net "USER_CLK"                  iostandard = LVCMOS33;       # Bank 2 Supply 3.3V
net "USER_TCLK"                 iostandard = LVCMOS33;       # Bank 2 Supply 3.3V


# Location Constraints
net "CLKGEN_SCL"                        loc = "J16";          # Bank 1
net "CLKGEN_SDA"                        loc = "J17";          # Bank 1
net "CLKGEN_INTR"                       loc = "C20";          # Bank 1

net "USER_CCLK"                         loc = "AB13";         # Bank 2
net "MCB_CLK"                           loc = "Y13";          # Bank 2
net "USER_CLK"                          loc = "U12";          # Bank 2
net "USER_TCLK"                         loc = "T12";          # Bank 2


# Additional Constraints
net "USER_CCLK"                   tnm_net = "USER_CCLK";
timespec "TS_USER_CCLK"                   = period "USER_CCLK" 32 MHz high 50 %;

net "MCB_CLK"                     tnm_net = "MCB_CLK";
timespec "TS_MCB_CLK"                     = period "USER_MCB_CLK" 62.5 MHz high 50 %;

net "USER_CLK"                    tnm_net = "USER_CLK";
timespec "TS_USER_CLK"                    = period "USER_CLK" 83.3325 MHz high 50 %;

net "USER_TCLK"                   tnm_net = "USER_TCLK";
timespec "TS_USER_TCLK"                   = period "USER_CCLK" 32 MHz high 50 %;


## ##############################################################################################
## Section: Debug
## ##############################################################################################

# Define I/O Standards
net "FPGA_?XD"                  iostandard = LVCMOS15;       # Bank 1 Supply 1.5V

net "FPGA_BUT"                  iostandard = LVCMOS15;       # Bank 1 Supply 1.5V


# Location Constraints
net "FPGA_RXD"                          loc = "L15";          # Bank 1
net "FPGA_TXD"                          loc = "K16";          # Bank 1

net "FPGA_BUT"                          loc = "D21";          # Bank 1


## ##############################################################################################
## Section: Module Management
## ##############################################################################################

# Define I/O Standards
net "FPGA_SW_n"                 iostandard = LVCMOS33;       # Bank 2 Supply 3.3V

net "FPGA_RST_n"                iostandard = LVCMOS33;       # Bank 2 Supply 3.3V
```

```
# Location Constraints
net "FPGA_SW_n"                         loc = "Y11";          # Bank 2

net "FPGA_RST_n"                        loc = "AA14";         # Bank 2


## ##############################################################################################
## Section: General Purpose I/O
## ##############################################################################################

# Define I/O Standards
net "GPIO_LED[?]"               iostandard = LVCMOS15;       # Bank 1 Supply 1.5V

net "GPIO_T*"                   iostandard = LVCMOS15;       # Bank 1 Supply 1.5V
net "GPIO_EN"                   iostandard = LVCMOS15;       # Bank 1 Supply 1.5V


# Location Constraints
net "GPIO_LED[0]"                       loc = "M16";          # Bank 1
net "GPIO_LED[1]"                       loc = "N15";          # Bank 1
net "GPIO_LED[2]"                       loc = "U19";          # Bank 1
net "GPIO_LED[3]"                       loc = "T20";          # Bank 1

net "GPIO_TCK"                          loc = "M17";          # Bank 1
net "GPIO_TMS"                          loc = "M18";          # Bank 1
net "GPIO_TDI"                          loc = "R15";          # Bank 1
net "GPIO_TDO"                          loc = "R16";          # Bank 1

net "GPIO_EN"                           loc = "P18";          # Bank 1
```